FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: **KSN0012**

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/806401

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE99/03247	**08 October 1999**	**09 October 1998**

TITLE OF INVENTION

ELECTRONIC MODULE, ESPECIALLY A MULTICHIP MODULE, WITH MULTI-LAYER METALLIZATION AND CORRESPONDING PRODUCTION METHOD

APPLICANT(S) FOR DO/EO/US

Harry Hedler, Gregor Feiertag, Peter Deml, and Franz Petter

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☐ Other items or information:

Check No. in the amount of $860.00, Copy of Change of Applicant

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/806401	PCT/DE99/03247	KSN0012

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1,000.00
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	$860.00
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$710.00
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$690.00
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	$0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	9 - 20 =	0	x $18.00	$0.00	
Independent claims	1 - 3 =	0	x $80.00	$0.00	
Multiple Dependent Claims (**check if applicable**).			☐	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$860.00	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) (**check if applicable**).			☐	$0.00	
SUBTOTAL =				$860.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				$0.00	
TOTAL NATIONAL FEE =				$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (**check if applicable**).			☐	$0.00	
TOTAL FEES ENCLOSED =				$860.00	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$860.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **02-0387** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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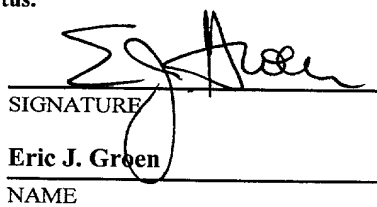
Telephone: (219) 234-4149
Fax: (219) 239-1900



SIGNATURE

Eric J. Groen
NAME

32,230
REGISTRATION NUMBER

March 30, 2001
DATE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Harry Hedler, Gregor Feiertag, Peter Deml, and Franz Petter

Filed: PCT/DE99/03247 October 8, 1999

For: ELECTRONIC MODULE, ESPECIALLY A MULTICHIP MODULE, WITH MULTI-LAYER METALLIZATION AND CORRESPONDING PRODUCTION METHOD

Commissioner for Patents and Trademarks
Washington DC 20231

Dear Sir:

PRELIMINARY AMENDMENT

In the above-mentioned PCT application, please accept the enclosed application under the national stage pursuant to 35 USC § 371 and amend the application as follows:

In the Claims:

Please replace claims 1-8 of the application with claims 1-9 as follows:

1. An electronic module, in particular a multichip module, comprising a multilayer wiring having at least one IC component applied on the component side thereof, said module being unilaterally covered on the component side with a hermetic case, and comprising contact pads on the bottom side of the module through for contacting and integration of the module to a next higher assembly group level, the bottom side of the multilayer wiring constituting directly, without additional wiring substrate, the bottom side of the module, the component side of the multilayer wiring adhering to the hermetic case with

its portions that are free from components, said hermetic case being formed by plastics overmolding, and in that the multilayer wiring has a height of less than approximately 100 µm.

2. A module according to claim 1, wherein the multilayer wiring is constituted by a sequence of structured metal planes which are electrically separated from each other by insulating layers and between which purposeful electric connections are established through vias.

3. A module according to claim 1, wherein solderable material is applied to the contact pads on the bottom side of the multilayer wiring, electrically connected to the component level through vias, for establishing contact with the next assembly group level.

4. A module according to claim 3, wherein the solderable material is applied in the form of solder balls

5. A method of making an electronic module according to claim 1, in which

- a multilayer wiring having contact pads on the bottom side thereof is applied only to the top side of a plate-shaped wiring substrate of rigid material,
- IC components and additional electronic components, respectively, are electrically and mechanically connected to the component level of the multilayer wiring,

the component side of the multilayer wiring is provided with a hermetic case adhering in the portions thereof that are free from components,

- the rigid substrate material is removed again thereafter and the bottom side of the multilayer wiring which constitutes the bottom side of the module, is exposed, and

said hermetic case is formed by unilateral plastics overmolding.

6. A method according to claim 4, wherein, prior to removal of the particular metallic substrate material in portions located underneath the contact pads, pits are etched into the wiring substrate from the bottom side, with solderable material being introduced into said pits thereafter.

7. A method according to claim 4, wherein the removal of the particular metallic substrate material takes place by dissolution of the same.

8. A method according to claim 7, wherein the dissolution takes place by wet chemical etching.

9. A method according to claim 4, wherein the removal of the substrate material takes place by stripping the wiring substrate from the multilayer wiring.

REMARKS

Applicants respectfully request that the above preliminary amendment be entered, and that the fees due herewith are calculated using the new claims, not the claims of the PCT application.

Respectfully submitted,

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Specification

Electronic Module, in Particular a Multichip Module, Comprising a Multilayer Wiring and Method of Making the Same

The invention relates to an electronic module, in particular a multichip module, comprising a multilayer wiring having at least one IC component applied on the component side thereof, said module being unilaterally covered on the component side with a hermetic case, and comprising contact pads on the bottom side of the module through which contacting and integration of the module to a next higher assembly group level can be established.

The invention moreover relates to a method of making an electronic module, in particular a multichip module, comprising a multilayer wiring.

The increasing reduction in size and growing speed of integrated circuits meets with increasing demands on the extension and connection technology thereof. Multichip modules have been known for some tome through which an intermediate carrier substrate with high wiring density, HDI (High Density Interconnect), is introduced into the hierarchy of the system structure as an additional level. Typical in this respect is the use of a plurality of unpackaged chips as well as a high area coverage of the multichip substrate. A similar known new development relates to the chip size package (CSP) in which a single unpackaged chip is applied to an intermediate carrier substrate which is hardly larger than the chip area and in which the space-saving contacting to the next architectural level directly under the chip area is utilized.

The essential features of today's packages for single-chip or multichip applications are the lateral dimension, the construction height, the heat dissipation and the pitch in the next architectural level. The utilization of the known quad flat pack (QFP) packages, in addition to the relatively low degree of chip coverage (chip area/component area) and the relatively high construction height, involves the additional disadvantage of the transition to extremely small pitches on the motherboard with high pincount of the chips. There is also known an additional package type, the ball grid arrays (BGA). In case of these, small solder balls applied over the area or in sheet-like manner on the bottom side of the module in a relatively coarse grid pattern, constitute the terminals. By means of BGA constructions, the arrangement of the contacts in sheet-like manner assists in mitigating the problems concerning the pitch, and the construction height can be reduced in principle. However, the manufacture of conventional laminate/plastics interconnects, in particular for high-density wirings, results in technical detours and disadvantageous product properties. In total, the current situation presents itself as follows:

The technologies of circuit board production render possible wiring substrates permitting electric through-contacting from the chip side to the bottom side by means of plated-through holes that can be made in relatively simple manner. They are less advantageous as regards the production of constructional shapes of small lateral dimensions, in particular for multichip modules, as the wiring densities are too low. Furthermore, in particular vias between the conductive track levels are not positioned in sufficiently exact manner due to the shrinkage of the laminate materials. There are left uncertainties of typically up to 200 µm, and this is brought to regis-

tration by a coarser design of the structure around the via (land). Due to the shrinkage, high-density wiring substrates can be realized only if the production is not carried out on the inexpensive large panels, for example of 600 x 600 mm, but on extremely small ones, for example of 150 x 150 mm. Large-format production in circuit board technology thus involves high costs comparable to those in thin-film technology.

The technologies of thin-film production permit high wiring densities due to their processes employing fine structures, and there is no shrinkage problem due to the rigid substrate materials (the substrate proper for the multilayer wiring consists of ceramic, silicon, glass or metal). However, there are problems arising with other aspects of this technology, in particular as regards the cost-intensive detours, such as drilling or punching holes in the rigid core materials, adjustment problems, metallization of the holes, etc., as necessary in realizing the electrical connection from the substrate top side to the substrate bottom side. In addition thereto, the density of the plated-through holes is restricted by the substrate thickness and the respective technology for making the hole. In general, there is poor compatibility between the technology of substrates with holes on the one hand and processes in thin-film technique, for example spin coating, on the other hand. Finally, there is also a high risk of breakage of the substrates in the thin-film process which moreover does not permit a simple change to inexpensive large-format production, either.

It is the object of the present invention to provide an improved module of the type indicated at the outset, having in particular a reduced construction height, and to indicate a method of making the same.

With a module of the type indicated at the outset, this object is met in that the component side of the multilayer wiring adheres to the hermetic case with its portions that are free from components, and in that the bottom side of the multilayer wiring having a height of less than approx. 100 µm, directly, i.e. without additional wiring substrate, constitutes the bottom side of the module.

With a method of the type indicated at the outset, the object is met in that a multilayer wiring having contact pads on the bottom side thereof is applied only to the top side of a plate-shaped wiring substrate of rigid material, that IC components and additional electronic components, respectively, are electrically and mechanically connected to the component level of the multilayer wiring, that the component side of the multilayer wiring is provided with a hermetic case adhering in the portions thereof that are free from components, and in that the rigid substrate material is removed again thereafter and the bottom side of the multilayer wiring, which constitutes the bottom side of the module, is exposed.

Further developments of the invention are subject matter of the dependent claims.

The invention will be elucidated in more detail hereinafter by way of embodiments in connection with the drawing figures in which

Figs. 1A to 1D show cross-sectional side views of successive stages of the manufacturing process according to the invention in a first embodiment,

Figs. 2A to 2F show corresponding views of another embodiment,

Figs. 3A to 3F show corresponding views in a further embodiment.

The invention achieves the desired improvements in that not only the processes of the interconnect production proper are taken into consideration, but in that the overall process for making a BGA standard package is incorporated in the rationalization and restructuring of the process sequences according to the invention and thus of the module itself. According to the invention, it is possible to produce ultra-thin modules although the utilization of the advantages of thin-film technique, i.e. in particular the use of rigid substrate materials or materials of high temperature stability (up to 400 °C) is maintained on the one hand, whereas on the other hand a high wiring density can be achieved in unrestricted manner and large-size panels, for example 400 x 400 mm, can be used for the production. In addition thereto, there is the advantage that process steps can be dispensed with.

Fig. 1A shows a metallic wiring substrate 1 having already applied on the top side thereof the interconnect proper, i.e. the multilayer wiring 2, which is constituted by a sequence of structured metal planes or levels that are electrically separated from each other by insulating layers and between which purposeful electric connections are established through vias. Suitable substrate materials are, for example, copper or aluminium. It is of crucial importance that the multilayer wiring 2 actually is applied on the substrate top side only and that there are no plated-through holes made from the top side to the bottom side of wiring substrate 1. Fig. 1 shows a module in which, compared with Fig. 1A, two additional production steps have been carried out, namely mechanical and electrical connection of one or more

chips 3 and, optionally, of additional electronic components to the component side of the multilayer wiring 2, for example by chip and wire bond technique or flip chip technique, with the equipped system being then brought into the configuration of a standard package by unilateral plastics molding (overmold), cp. case 4. The largest part of the component area, i.e. of the top side of the multilayer wiring 2, is free from components so that the casting or adhesive compound 4 applied can establish sufficient adhesive areas 5 towards the multilayer wiring 2. In particular, the usual casting compounds may be employed as these are compatible anyway, i.e. capable of adhering, to the insulating materials used as uppermost layer of the multilayer wiring 2, such as polyimide, PBO, BCB or ormocere.

Fig. 1C shows a module in which the next process step, the removal of the substrate material 1, has already been carried out. This can be achieved, for example, by dissolution of the substrate material, in particular by wet chemical etching in one of the etch plants usual in the trade, as used for example in high-integration semiconductor technology. Thereafter and due to this, the contact pads 6 on the bottom side of the multilayer wiring 2, which by means of vias and connections to the conductive track system are to ensure the electrical contact of the components 3 of the module to the contacts of the next higher assembly group level, of course are exposed as well. As shown in Fig. 1D, this is usually followed by the application of solderable material, in particular soldering balls 7, to the contact pads 6 for establishing contact to the module. A passivation layer 15 may be provided to permit easier testing of the module later on, cp. Fig. 1B. Basically, e.g. plastics material is possible as substrate material as well.

While Figs. 2A and 2B correspond to the manufacturing steps according to Fig. 1A and 1B, Figs. 2C and 2F show embodiments differing therefrom. Fig. 2C shows the result of etching pits 8 into the substrate material from the bottom side, so that the contact locations, i.e. the contact pads 6 on the bottom side of the multilayer wiring 2 are exposed. Thereafter, solderable material 9 (e.g. SnPb) can be introduced into the pits 8 by electroplating, or solder balls 7 can be introduced into the pits 8 by standard processes, cp. Fig. 1D. Only thereafter is the removal of the wiring substrate 1 carried out, with modules according to Fig. 2E or 2F being the final result depending on the type of solder material 8, 9 chosen.

As an alternative to the removal of the substrate material by dissolution as described hereinbefore, another suitable possibility of separation consists in stripping the wiring substrate 1 from the multilayer wiring 2. This can be realized in particular by application of an intermediate layer between multilayer wiring 2 and wiring substrate 1. For example, a low melting point material, e.g. solder, or an adhesive is well suited, which at the end of the molding process permits separation of the module from the wiring substrate 1, for example, by means of an additional heat treatment step. Figs. 3A to 3E display a process sequence in which a solder layer 10 as intermediate layer is applied to the substrate material first, which then is covered with a structured insulating layer 11. According to Fig. 3C a structured metal plane 12 is made, which according to Fig. 3D is equipped with electronic components and covered by a hermetic case 4. Fig. 3E shows the final result after heating of the solder layer 10 and removal of the wiring substrate 1, with harmless residues of the solder layer 10 being left at the solder pads 10, and only there. Within the conductive track system of the multilayer

wiring 2, which in this special case permitting particularly inexpensive production consists of one single metal and one single insulating layer 12 and 11 only, the metal lands 13 and 14 are connected to each other. When an adhesive is used as intermediate layer, care should be taken that the same is as residue-free as possible, or post-cleaning should be provided for.

According to the invention, the result achieved consists in a module in the form of a BGA standard package having an extremely low assembly height, since the sole remaining multilayer wiring 2, the interconnect proper, has an assembly height of less than approx. 100 µm, mostly even less than 60 µm. Due to the fact that the chips 3 in thinned form typically have a height of approx. 300 µm and the hermetic case 4 once more takes a similar height, minimum package heights (without balls) of approx. 600 µm can be achieved according to the invention, whereas for example in laminate technology the known interconnect alone, i.e. the wiring substrate with the multilayer wiring arranged thereon has a height between 500 µm and 1000 µm.

Translation of Amended Pages

Claims

1. An electronic module, in particular a multichip module, comprising a multilayer wiring having at least one IC component applied on the component side thereof, said module being unilaterally covered on the component side with a hermetic case, and comprising contact pads on the bottom side of the module through which contacting and integration of the module to a next higher assembly group level can be established, the bottom side of the multilayer wiring (2) constituting directly, i.e. without additional wiring substrate (1), the bottom side of the module,
characterized in
that the component side of the multilayer wiring (2) adheres to the hermetic case (4) with its portions that are free from components, said hermetic case (4) being formed by plastics overmolding, and in that the multilayer wiring (2) has a height of less than approx. 100 µm.

2. A module according to claim 1,
characterized in that the multilayer wiring (2) is constituted by a sequence of structured metal planes (12) which are electrically separated from each other by insulating layers (11) and between which purposeful electric connections are established through vias.

3. A module according to claim 1 or 2,
characterized in that, for establishing contact with the next assembly group level, solderable material

(7, 9), in particular solder balls (7), are applied to the contact pads (6) on the bottom side of the multilayer wiring (2) which are electrically connected to the component level through vias.

4. A method of making an electronic module according to claim 1, in which

- a multilayer wiring (1) having contact pads (6) on the bottom side thereof is applied only to the top side of a plate-shaped wiring substrate (1) of rigid material,
- IC components and additional electronic components (3), respectively, are electrically and mechanically connected to the component level of the multilayer wiring (2),
- the component side of the multilayer wiring (2) is provided with a hermetic case (4) adhering in the portions thereof that are free from components,
- and the rigid substrate material is removed again thereafter and the bottom side of the multilayer wiring (2), which constitutes the bottom side of the module, is exposed,

characterized in
that said hermetic case is formed by unilateral plastics overmolding.

5. A method according to claim 4,
characterized in that, prior to removal of the in particular metallic substrate material in portions located underneath the contact pads (6), pits (8) are etched into the wiring substrate (1) from the bottom side, with solderable material (7, 9) being introduced into said pits (8) thereafter.

6. A method according to claim 4 or 5,

characterized in that the removal of the in particular metallic substrate material takes place by dissolution of the same.

7. A method according to claim 6,
characterized in that the dissolution takes place by wet chemical etching.

8. A method according to claim 4 or 5,
characterized in that the removal of the substrate material takes place by stripping the wiring substrate (1) from the multilayer wiring (2).

FIG 1 A

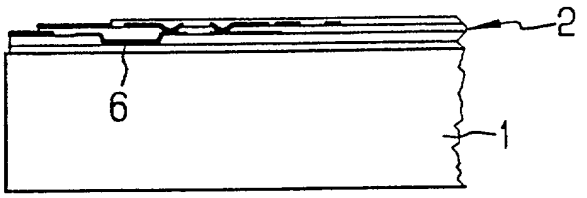


FIG 1 B

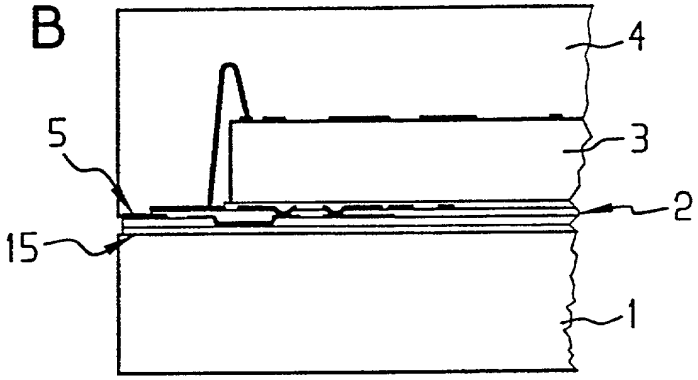


FIG 1 C

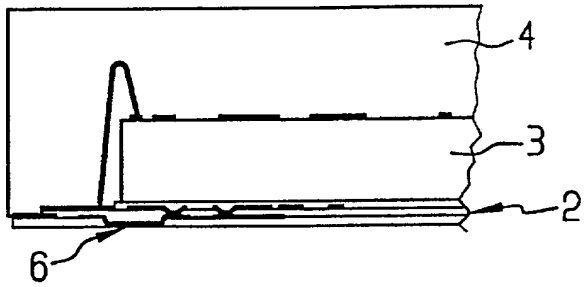


FIG 1 D

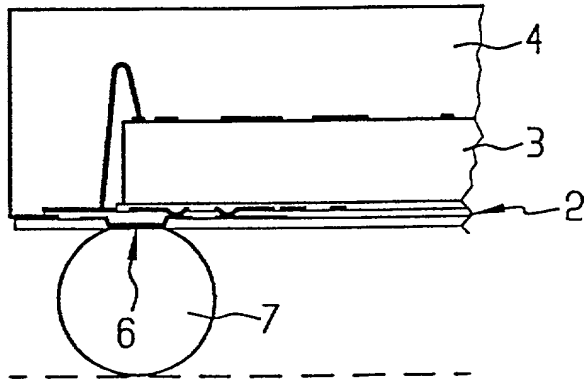


FIG 2 A

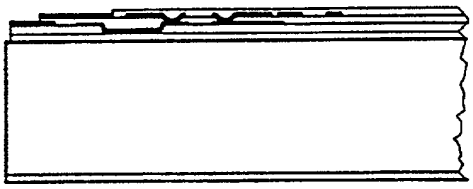


FIG 2 B

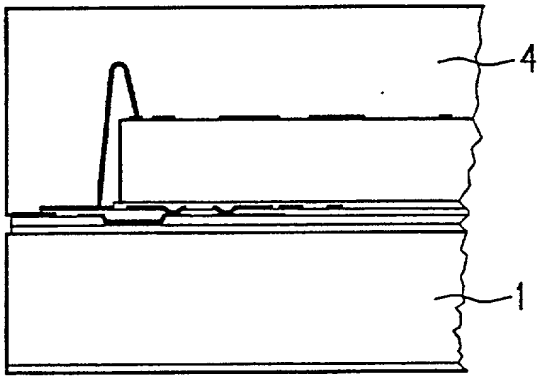


FIG 2 C

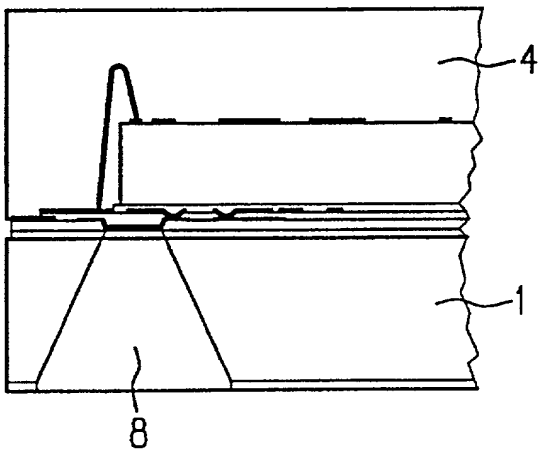


FIG 2 D

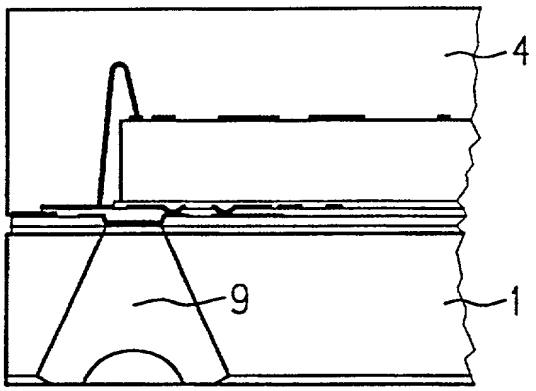


FIG 2 E

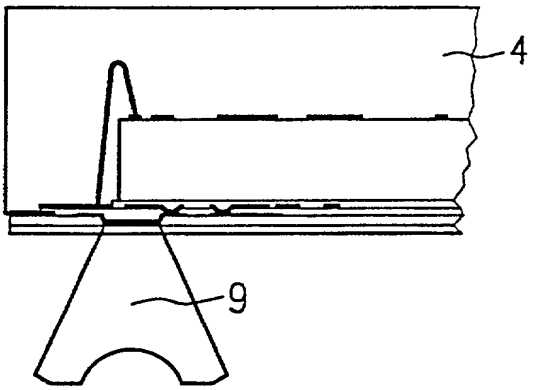


FIG 2 F

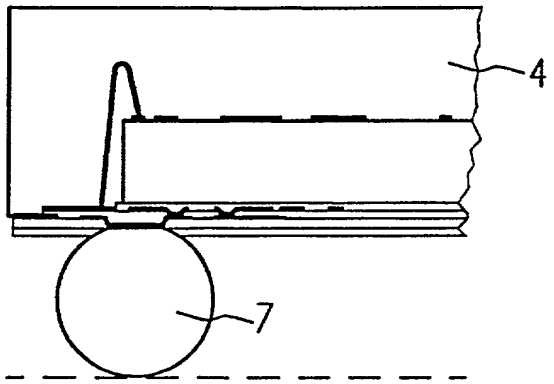


FIG 3A

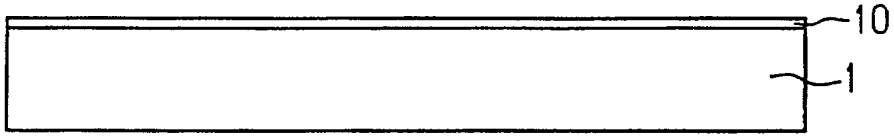


FIG 3B

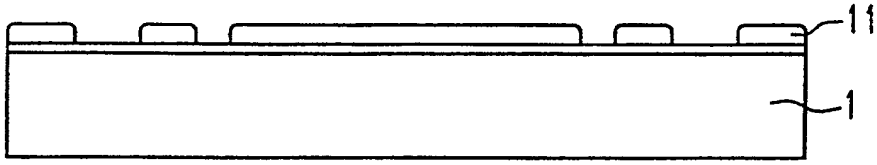


FIG 3C

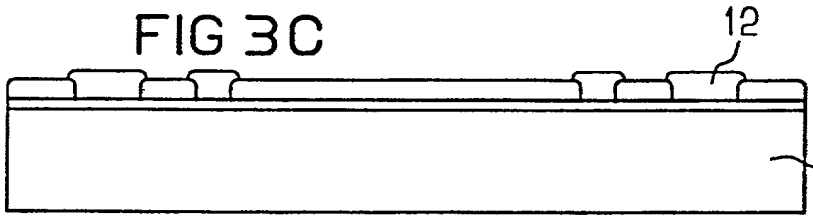


FIG 3D

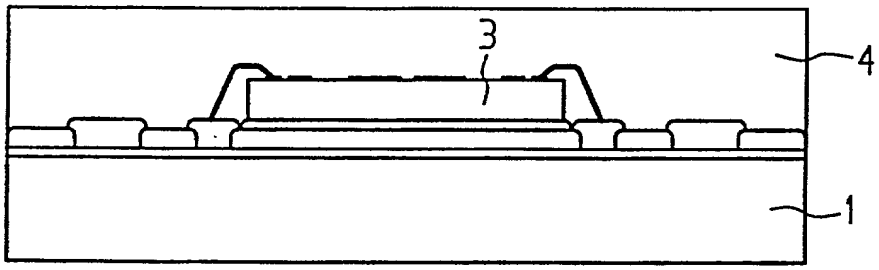
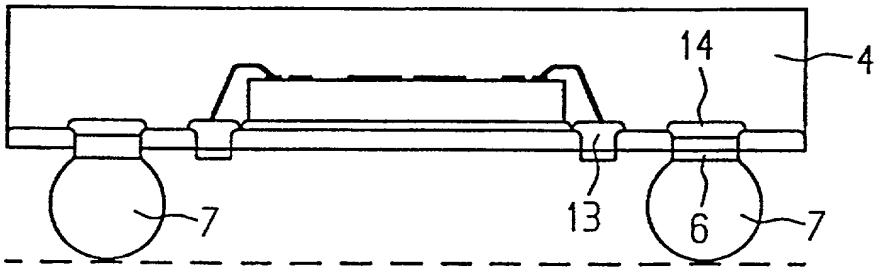


FIG 3E



Docket No.
KSN0012

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

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the specification of which

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and was amended on _____
(if applicable)

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DE 198 46 662.5	**Germany**	**9 October 1998**	☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	
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PCT/DE99/03247	**8 October 1999**	**Pending**
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
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205 West Jefferson Blvd., Suite 250
South Bend, IN 46601

Direct Telephone Calls to: *(name and telephone number)*
Eric J. Groen (219)234-4149

Full name of sole or first inventor **Harry Hedler**
Sole or first inventor's signature — Date 30-05-01
Residence ~~**Pelargonienweg 50 A, D-81377 Munchen**~~, **Germany** Jahnstrasse 8, D-82110 Germering DEX
Citizenship **German** Harry Hedler
Post Office Address ~~**Pelargonienweg 50 A, D-81377 Munchen**~~, **Germany** Jahnstrasse 8, D-82110 Germering

Full name of second inventor, if any **Gregor Feiertag**
Second inventor's signature — Date
Residence **Ruffinistrasse 22, D-80637 Munchen, Germany** DEX
Citizenship **German**
Post Office Address **Ruffinistrasse 22, D-80637 Munchen, Germany**

Full name of third inventor, if any **Peter Deml**
Third inventor's signature Date
Residence **Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany** DEX
Citizenship **German**
Post Office Address **Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany**

Full name of fourth inventor, if any **Franz Petter**
Fourth inventor's signature Date
Residence ~~**Hohenweg** 20, D-85247 **Schwabhausen,**~~ **Germany** Hoehenweg 20, D-85247 Oberroth DEX
Citizenship **German**
Post Office Address ~~**Hohenweg** 20, D-85247 **Schwabhausen,**~~ **Germany** Hoehenweg 20, D-85247 Oberroth

Full name of fifth inventor, if any
Fifth inventor's signature Date
Residence
Citizenship
Post Office Address

Full name of sixth inventor, if any
Sixth inventor's signature Date
Residence
Citizenship
Post Office Address

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Full name of sole or first inventor **Harry Hedler**
Sole or first inventor's signature Date
Residence ~~**Pelargonienweg 50-A, D-81377 Munchen**~~, **Germany** Jahnstrasse 8, D-82110 Germering
Citizenship **German**
Post Office Address ~~**Pelargonienweg 50-A, D-81377 Munchen**~~, **Germany** Jahnstrasse 8, D-82110 Germering

Full name of second inventor, if any **Gregor Feiertag**
Second inventor's signature Date May 27, 2007
Residence **Ruffinistrasse 22, D-80637 Munchen, Germany**
Citizenship **German**
Post Office Address **Ruffinistrasse 22, D-80637 Munchen, Germany**

Full name of third inventor, if any
Peter ~~Deml~~

Third inventor's signature Date

Residence
Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany

Citizenship
German

Post Office Address
Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany

Full name of fourth inventor, if any
Franz Petter

Fourth inventor's signature Date

Residence
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Citizenship
German

Post Office Address
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Full name of fifth inventor, if any

Fifth inventor's signature Date

Residence

Citizenship

Post Office Address

Full name of sixth inventor, if any

Sixth inventor's signature Date

Residence

Citizenship

Post Office Address

Docket No.
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Sole or first inventor's signature Date
Residence ~~**Pelargonienweg 50 A, D-81377 Munchen**~~, **Germany** Jahnstrasse 8, D-82110 Germering
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Second inventor's signature Date
Residence **Ruffinistrasse 22, D-80637 Munchen, Germany**
Citizenship **German**
Post Office Address **Ruffinistrasse 22, D-80637 Munchen, Germany**

Full name of third inventor, if any **Peter Deml**
Third inventor's signature Date 6.7.01
Residence **Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany**
Citizenship **German**
Post Office Address **Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany**

Full name of fourth inventor, if any **Franz Petter**
Fourth inventor's signature Date
Residence **~~Hohenweg~~ 20, D-85247 ~~Schwabhausen~~, Germany** Hoehenweg 20, D-85247 Oberroth
Citizenship **German**
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Fifth inventor's signature Date
Residence
Citizenship
Post Office Address

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Sixth inventor's signature Date
Residence
Citizenship
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Harry Hedler

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Full name of second inventor, if any
Gregor Feiertag

Second inventor's signature — Date
May 23, 2007

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Citizenship
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Full name of third inventor, if any
Peter Deml

Third inventor's signature

Date
6.7.01

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Full name of fourth inventor, if any
Franz Petter

Fourth inventor's signature

Date
8.10.2001

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German

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Full name of fifth inventor, if any

Fifth inventor's signature

Date

Residence

Citizenship

Post Office Address

Full name of sixth inventor, if any

Sixth inventor's signature

Date

Residence

Citizenship

Post Office Address